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Title: PROGRAMMABLE JITTER SIGNAL GENERATOR

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PROGRAMMABLE JITTER SIGNAL GENERATOR

BACKGROUND OF THE INVENTION

The present invention relates generally to the testing of timing jitter, and in particular, to an apparatus and method for providing a programmable jitter signal generator. Timing jitter is defined as the short-term deviation in significant instants of digital signals as referenced to their equidistant normal instants.

As shown in Figure 1, an exemplary plot of jitter is indicated generally by the reference numeral 100. The solid square wave 110 represents a jitter-free reference signal where the rising edges and falling edges are equally distant from each other. The dashed square waves 112 and 114 are signals with early transition and late transition jitter, respectively. By comparing the timing instant of the rising edges or falling edges between these signals and the reference signal 110, it can be seen there are timing deviations. These timing deviations are called timing jitter.

In today's high-speed computing and communications systems, jitter is a crucial parameter. It is important for such systems to minimize the impact from the timing jitter, and to tolerate a certain level of timing jitter in the input signal while maintaining performance. Accordingly, high-speed computing and communications system must be tested for their tolerance to jitter.

Turning to Figure 2, a test setup for testing system jitter tolerance ability is indicated generally by the reference numeral 200. The setup 200 includes three blocks, a jitter signal generator 210, a system under test 212 in signal communication with the generator 210, and a system response analyzer 214 in signal communication with the system 212.

In operation of a test, the jitter signal generator 210 generates a signal with known jitter and applies it to the system under test 212. The output of the system under test is its response to the input with jitter. This response is passed into the system response analyzer block 214, where the system jitter tolerance is evaluated.

To conduct the jitter tolerance test, the type of jitter signal generator used is of paramount importance. It should be able to generate jitter in a controllable fashion and then deliberately inject the jitter into the data stream. A traditional method uses a frequency modulation ("FM") technique to modulate a low frequency sinusoidal signal onto a carrier frequency sinusoidal signal, which in turn triggers a pulse generator. In this method, most of the jitter parameters cannot be controlled, such as jitter distribution, jitter amplitude and the like. Thus, the system's jitter tolerance characteristics cannot be evaluated completely and accurately.

For instance, in phase locked loop ("PLL") testing, the transfer function and input jitter caused output jitter cannot be easily determined. Similarly, in high-speed transceiver and A/D converter testing, jitter tolerance cannot be completely tested. Accordingly, what is needed is a controllable jitter generation technique to overcome these and other drawbacks and disadvantages of the prior art.

SUMMARY OF THE INVENTION

The above and other drawbacks and deficiencies of the prior art are overcome or alleviated by a programmable jitter signal generator.

A programmable jitter signal generator is provided that includes a jitter distribution control unit, a selection unit in signal communication with the jitter distribution control unit, and a delay unit in signal communication with the selection unit; and a corresponding method of generating a programmable jitter signal includes programming a control unit, receiving a reference signal, delaying the received reference signal by a multiple of a base time increment, and selecting a delayed reference signal delayed by a desired multiple of the base time increment in accordance with the programmed control unit.

These and other aspects, features and advantages of the present disclosure will become apparent from the following description of exemplary

embodiments, which is to be read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may be better understood with reference to the following exemplary figures, in which:

Figure 1 shows a plot of ideal and jitter waveforms;

Figure 2 shows a block diagram of a jitter testing system;

Figure 3 shows a circuit diagram of a programmable jitter signal generator in accordance with a preferred embodiment of the present disclosure;

Figure 4 shows plots of signal delays in accordance with a voltage-controlled delay chain of Figure 3;

Figure 5 shows a circuit diagram of a first exemplary jitter distribution control block in accordance with Figure 3;

Figure 6 shows a circuit diagram of a second exemplary jitter distribution control block in accordance with Figure 3; and

Figure 7 shows a modified delay chain circuit in accordance with Figure 3.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A programmable jitter signal generator and method are provided herein. Embodiments of the programmable jitter signal generator may be used in a test setup as described in Figure 2. Preferred embodiments of the programmable jitter signal generator are able to generate jitter in a controllable fashion and then deliberately inject the jitter into a data stream, while controlling jitter parameters such as jitter distribution, jitter amplitude and the like, to thereby enable complete and accurate evaluation of a system's jitter tolerance characteristics.

As shown in Figure 3, an exemplary programmable jitter signal generation circuit is indicated generally by the reference numeral 300. The circuit 300 includes a delay chain 310 to adjust the time instants of the rising edge of a jitter-free reference signal. A jitter distribution control block 312 and multiplexer or signal selector 314 are used to select a delay cell for delayed output. Here, the selector 314 is a 32:1 selector, which is in signal communication with each cell of the delay chain 310 and the control block 312. The data distribution in the jitter distribution control block is programmable, and the delay time of the delay cells is also controllable. Therefore, the circuit can create a signal with controllable average jitter, RMS jitter, peak-to-peak jitter, and cycle-to-cycle jitter, which can meet most

system test requirements. In addition, the circuit can be integrated onto the circuit of interest for built in self-test ("BIST") applications.

In operation of the circuit 300, the input reference signal Sin enters the delay chain 310 from the left. Sin is a timing signal with very low jitter, such as can be obtained from conventional test equipment. The exemplary delay chain 310 includes 32 delay cells or delay buffers 311, each of which delays the signal by an amount t1. Note that 32 elements are chosen for illustrative purposes, but that any number of delay elements may be included in alternate embodiments to meet application requirements. When the reference signal, Sin, goes through each delay buffer, its rising edge instant will be deviated by time t1.

Turning to Figure 4, a plot of delay increments achievable with the delay chain 310 of Figure 3 is indicated generally by the reference numeral 400. If the phase of the central cell 311 of Figure 3 has output referred to as 0, then the whole delay chain could generate timing edges with delays ranging from -15*t1 to 16*t1, which are indicated by the reference numerals 410 through 441, respectively. By changing the length of the delay chain, this jitter amplitude range could be adjusted correspondingly. By adjusting the delay control voltage, the interval t1 can be adjusted to further adjust the jitter distribution. If time intervals smaller than t1 are required, an additional

multiplexer with cell delays t2...tn can be added and the Sout of each multiplexer can be fed to an additional final multiplexer.

The output of each delay cell 311 is connected to the corresponding input of a multiplexer or signal selector 314. The five signals a4, a3, a2, a1 and a0 are used to select a signal from the appropriate delay cells and connect it with the output terminal Sout.

The jitter control block 312 of Figure 3 controls jitter distribution and magnitudes of average jitter, Root Mean Square ("RMS") jitter, peak-to-peak jitter and cycle-to-cycle jitter in the generated signal with jitter, Sout. By setting the data distribution of a4, a3, a2, a1 and a0, the jitter distribution is controlled. The data distribution and the interval t1 are used to calculate the generated average jitter, RMS jitter and peak-to-peak jitter. The cycle-to-cycle jitter equals t1 times any two a4a3a2a1a0 sequences.

Turning now to Figure 5, an exemplary jitter distribution control block 312 of Figure 3 is indicated generally by the reference numeral 500. The jitter distribution control block 500 includes a random number generator 510, a random access memory ("RAM") array 512 in signal communication with the generator 510, and a binary counter 514 in signal communication with the RAM array 512.

The design of a jitter distribution control block may follow one of two design schemes. In the first scheme, patterns that create the desired jitter distribution are stored in the RAM, and applied to the multiplexer control signals. In the exemplary jitter distribution control block 500 of Figure 5, for example, an 8-bit binary counter is utilized. This counter is triggered by the input clock signal CLK, and its output bus [Q7...Q0] is connected to the memory array's address bus [A7...A0]. With the arrival of each CLK's rising edge, the data on the bus [Q7...Q0] is increased by 1, which enables each memory unit to be accessed sequentially. This method provides the greatest flexibility to control the timing jitter.

As shown in Figure 6, a circuit implementation of a second jitter distribution control design scheme is indicated generally by the reference numeral 600. The second jitter distribution control circuit 600 includes five D-type flip-flops ("DFF"), 610, 616, 622, 628 and 634, respectively, connected in series signal communication with summing units 612, 618, 624 and 630 therebetween, respectively. Multipliers 614, 620, 626 and 632 are applied to second inputs of each of the summing units, respectively. The output signals a0, a1, a2, a3 and a4 are the respective outputs of each of the DFFs 610 through 634, respectively.

The second jitter distribution control circuit 600 uses this hardware to generate pseudorandom data. In this scheme, linear feedback shift registers ("LFSR") are used to generate pseudorandom numbers. Thus, in the LFSR as is shown in Figure 6, five DFFs are connected in series to form a pseudorandom number generator. Once the LFSR is triggered, the signal will be shifted from one bit to the next significant bit. At every tap, a weight bit Ci is set to control the feedback from the most significant bit ("MSB"). If the seeds of the LFSR are known, the patterns will be yielded in certain order. In this method, since one can deduce all the random patterns from the LFSR seed, the memory isn't needed to store the generated numbers, simplifying the design.

Turning to Figure 7, a modified delay chain circuit is indicated generally by the reference numeral 700. The circuit 700 includes a first AND gate 710 and a second AND gate 712. The second AND gate 712 has a first input terminal for receiving a signal Sin, and a second input terminal for receiving a signal Normal/Test. An inverter 714 is in signal communication between the second input of the second AND gate 712 and a first input of the first AND gate 710. An OR gate 716 is in signal communication with each of the AND gates, receiving the output of the AND 710 on its first input, and receiving the output of the AND 712 on its second input. The output of the

OR gate is in signal communication with the Sin input of a delay chain 718, which is comparable to the previously described delay chain 310 of Figure 3. The delay chain 718 further receives a voltage control signal Vcnt to control the time constants of the delay cells. The output of the delay chain 718 is in signal communication with an inverting cell 720 to provide negative feedback for the modified delay chain circuit 700, which forms an oscillating chain. The inverting cell 720 receives the signal Vcnt as its time constant control input, and outputs a signal Stest. The signal Stest is provided as negative feedback to the second input of the first AND gate 710.

The clock input to the jitter distribution control block determines the rate at which the signals from the delay cell are selected, thereby determining the bandwidth of the jitter of the final signal, Sout. The delay cell chain can be designed in many ways. The major feature is that each cell's delay time t1 should be controllable. Thus, the timing jitter resolution will be adjustable. During each jitter generation process, the delay time t1 of each delay cell should be known. To be able to measure t1, the structure of the delay chain is modified as shown in Figure 7.

In this modified chain 700, an inverter 720 is added at the end of the original delay chain 718 (or 310 of Figure 3). This inverter 720 has the exact same structure and size as inverters in the delay buffers. The other four

basic logic gates (two AND gate, one OR gate, and one inverter) are applied to set the delay chain into a normal jitter generation mode or into a chain test mode. In the jitter generation mode, a normal/test signal is 1. While in the test mode, the normal/test signal is 0, wherein all delay cells are connected as a ring oscillator. By measuring the frequency of signal Stest, the delay time t1 can be calculated. Since it is known that the delay chain contains n delay buffers, each buffer's delay time is t1 and the last single inverter's delay time is 0.5*t1. Therefore, the frequency of the signal Stest is:

$$f = \frac{1}{2*(n+0.5)*t_1} \qquad \text{(Eqn. 1)}$$

Thus, the delay time of the signal Stest is:

$$t_1 = \frac{1}{2*f*(n+0.5)} \qquad \text{(Eqn. 2)}$$

Although illustrative embodiments have been described herein with reference to the accompanying drawings, it is to be understood that the present invention is not limited to those precise embodiments, and that

various changes and modifications may be effected therein by one of ordinary skill in the pertinent art without departing from the scope or spirit of the present invention. All such changes and modifications are intended to be included within the scope of the present invention as set forth in the appended claims.